Claims

[c1] A method of fabricating a gate structure of an integrated circuit, comprising:
forming a metal-containing gate in an opening within a dielectric region formerly occupied by a sacrificial gate, said metal-containing gate including:
a first layer consisting essentially of at least one selected from the group consisting of a metal and a metal compound, said first layer contacting a gate dielectric, the gate dielectric contacting a transistor channel region formed in a semiconductor region of a substrate;
a diffusion barrier layer overlying said first layer; and
a second layer consisting essentially of a metal overlying said diffusion barrier layer.

[c2] The method of claim 1 wherein said first layer consists essentially of at least one material selected from the group consisting of iridium (Ir), niobium (Nb), platinum (Pt), rhenium (Re), rhodium (Rh), ruthenium (Ru), tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tungsten (W), and vanadium (V).

[c3] The method of claim 2 wherein said second layer consists essentially of at least one material selected from the

group consisting of iridium (Ir), niobium (Nb), platinum (Pt), rhenium (Re), rhodium (Rh), ruthenium (Ru), tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tungsten (W), vanadium (V), Ni silicide, Co silicide and Ti silicide.

[c4] The method of claim 3 wherein at least one of said first layer and said second layer includes an impurity concentration to adjust said metal gate to a desired workfunction.

[c5] The method of claim 4 wherein said first layer consists essentially of tungsten deposited from a $W(CO)_6$ precursor and said second layer consists essentially of tungsten deposited from a WF_6 precursor.

[c6] The method of claim 1 further comprising depositing a layer of adhesion material prior to forming said diffusion barrier layer.

[c7] The method of claim 6 wherein said diffusion barrier layer consists essentially of titanium nitride (TiN) and said adhesion material consists essentially of titanium (Ti).

[c8] The method of claim 1 wherein said diffusion barrier layer includes at least one of a nitride of titanium, a nitride of hafnium and a nitride of zirconium.

[c9] The method of claim 8, wherein said diffusion barrier layer is formed by depositing TiN after depositing titanium.

[c10] The method of claim 8 wherein said diffusion barrier layer consists essentially of TiN.

[c11] The method of claim 1 wherein said dielectric region includes a pair of spacers disposed at sidewalls of said opening.

[c12] The method of claim 1 wherein said substrate is selected from the group consisting of a bulk semiconductor substrate, semiconductor-on-insulator substrate, silicon-on-insulator substrate, silicon germanium substrate and germanium substrate.

[c13] The method of claim 1 wherein said semiconductor region includes a thin film of semiconductor having a polycrystalline or amorphous form.

[c14] The method of claim 1 wherein said sacrificial gate is removed from the opening by etching and said method further comprises removing an etch stop layer disposed between the sacrificial gate and the semiconductor region and thereafter forming the gate dielectric.

[c15] The method of claim 14 wherein the gate dielectric has a

different thickness than the etch stop layer.

[c16] The method of claim 15, wherein said etch stop layer consists essentially of a layer of oxide.

[c17] The method of claim 1, wherein said sacrificial gate consists essentially of polysilicon.

[c18] The method of claim 1, wherein said first layer is thinner than said second layer and said first layer is between 2 nm and 20 nm thick.

[c19] The method of claim 18, wherein said first layer is between 2 nm and 10 nm thick.

[c20] The method of claim 1, wherein said first layer is deposited using a chemical vapor deposition (CVD) process.

[c21] The method of claim 20, wherein said first layer is depositing using a carbonyl of a metal as a deposition precursor.

[c22] The method of claim 21 wherein said diffusion barrier layer is annealed before forming the second layer.

[c23] The method of claim 22 further comprising the step of annealing said diffusion barrier at a temperature ranging between 400 and 600 degrees Celsius.

[c24] The method of claim 23, wherein said second layer is deposited using a chemical vapor deposition (CVD) process.

[c25] The method of claim 24 wherein said second layer is deposited using a fluorine containing compound gas of a metal as a deposition precursor.

[c26] The method of Claim 25 wherein said first layer of metal is deposited from a carbonyl containing precursor and said second layer of metal is deposited from a fluorine containing precursor.

[c27] The method of claim 1 wherein said dielectric region includes an interlevel dielectric layer extending from sides of said spacers over said semiconductor region and said metal gate is further planarized to a level of said interlevel dielectric layer.

[c28] The method of claim 27 wherein said planarization is conducted by chemical mechanical polishing.

[c29] A method of making a metal gate structure on a substrate comprising:
forming an etch stop layer on a semiconductor region of a substrate;
forming a sacrificial gate on said etch stop layer;

providing a pair of dielectric spacers on sidewalls of said sacrificial gate;
forming a dielectric layer on said substrate having a top surface generally planar to a top of said sacrificial gate;
removing said sacrificial gate to form an opening between said spacers;
removing said etch stop layer from under said opening;
forming a gate dielectric on said semiconductor region under said opening;
depositing a first layer of metal in said opening contacting said gate dielectric and sidewalls of said spacers;
forming a diffusion barrier layer on said first layer in said opening; and
depositing a second layer of metal on said diffusion barrier layer in said opening.

[c30] An integrated circuit including a transistor having a metal gate, said metal gate comprising:
a first layer of metal contacting a gate dielectric formed on a semiconductor region of a substrate;
a diffusion barrier layer overlying said first layer of metal; and
a second layer of metal overlying said diffusion barrier, said first and second layers of metal and said diffusion barrier layer being disposed within an opening between a pair of dielectric spacers.